REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 18, 2001, and the references cited therewith.

Claims 19, 20, 79, 81, 82, 84, 85, 104-106, 113, 115 and 117 are amended, and claims 119-124 are added; as a result, claims 19, 20, 53, 79-87, and 98-124 are now pending in this application.

§112 Rejection of the Claims

Claims 79, 82, 83, 86, 104, 105, 106, 113, 114, 115, 116, 117, and 118 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 79, 82, 85, 104, 105 and 106 have been amended such that the Markush group of metals refers to the metal layer rather than to the first conductive plate. Claims 115 and 117 have been amended to more specifically limit the material making up the "first conductive plate" (claim 115) and the "first capacitor electrode" (claim 117) instead of the metal layer, since limits on the material making up the metal layer have been added by virtue of amending claims 105 and 106.

Support for the metal layer comprising the listed group of metals can be found in the specification on page 5, lines 6-9, and on page 8, lines 20-27. Thus, the claims as amended satisfy the requirements of 35 USC § 112, first paragraph. Further, the amendments to the above-identified claims render the claims depending therefrom patentable in view of 35 USC § 112, first paragraph. Accordingly, Applicant requests withdrawal of the rejection of claims 79, 82, 83, 86, 104, 105, 106, 113, 114, 115, 116, 117, and 118 under 35 USC § 112, first paragraph.

§102 Rejection of the Claims

U.S. Patent No. 6, 051,885 to Yoshida

Claims 19, 53, 79, 81, 85, and 87 were rejected under 35 USC § 102(e) as being anticipated by Yoshida (U.S. Patent No. 6,051, 885). This rejection is understood to be based on the premise that Yoshida discloses a capacitor structure comprising: a first conductive plate (12), a metal layer (18) formed atop the first conductive plate, a second conductive plate (24) formed atop the first conductive plate, and a dielectric layer (22, a metal oxide formed by oxidizing the metal layer) formed between the first and second conductive plates.

Applicant makes no admission that Yoshida constitutes prior art, and reserves the right to to swear behind this reference. Nevertheless, Applicant believes the claims are patentably distinct from Yoshida for the reasons discussed below.

In Yoshida, conductor 12 is a substrate upon which the capacitor structure is formed and does not serve as one of the capacitor plates. Rather, the metal layer 18 serves as the lower capacitor plate, while the conductor 24 serves as the upper capacitor plate. Dielectric 22 is the insulation layer between metal layer 18 and conductor 24 (see e.g., col. 4, lines 22-26).

Claim 19 has been amended to clarify that the first and second conductive plates are capacitor plates, and that the metal oxide between the capacitor plates is formed from a metal layer of a different material than that of the first conductive plate. Because the metal oxide in claim 19 is not that formed by oxidizing the lower capacitor plate 25 (FIGS. 3-5), claim 19 is not anticipated by Yoshida. Accordingly, Applicant respectfully requests the anticipation rejection as to claim 19 be withdrawn. As claims 79 and 81 depend from claim 19 and further define various embodiments of the invention above the prior art, Applicant requests the anticipation rejection be withdrawn for these claims as well.

Claim 53 already includes limitations that distinguish it from Yoshida. In particular, the limitation that the "dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode" distinguishes Applicant's claimed invention from Yoshida. In Yoshida, the first capacitor electrode itself is oxidized, whereas in Applicant's claimed invention a separate metal layer overlying the first capacitor electrode is oxidized. Thus, Applicant's claimed invention allows for the dielectric layer to be a metal oxide different from that formed by oxidizing the first

capacitor electrode. Accordingly, claim 53 as well as claims 85 and 87 depending therefrom are not anticipated by Yoshida under 35 USC § 102(e). Applicant therefore respectfully requests withdrawal of the rejection of these claims.

B. U.S. Patent No. 5,876,788 to Bronner

Claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 were rejected under 35 USC § 102(a) as anticipated by Bronner, et al. (U.S. Patent No. 5,876,788).

Applicant makes no admission that Bronner constitutes prior art, and reserves the right to to swear behind this reference. Nevertheless, Applicant believes the claims are patentably distinct from Bronner for the reasons discussed below.

Bronner is directed to forming the structure shown in FIG. 1(e), as evidenced by the statement in col. 5, lines 21-23 (emphasis added), "The oxidized composite dielectric structure, *which represent the final composite dielectric structure of the present invention,* is shown in FIG. 1(e)." The structure shown in FIG. 1(e) of Bonner constitutes a semiconductor substrate 12 and a layer 14 that includes an upper metal oxide layer 22 interdiffused with a layer of Si_3N_4. Thus, layer 14 constitutes a composite dielectric structure designed to have a high dielectric constant and is not itself a capacitor structure. In any event, Applicant's claimed invention does not include the composite dielectric structure of Bronner as part of the claimed capacitor structure.

The structure of FIG. 1(b) cited by the Examiner is an intermediate structure that arises on the way to forming the final composite dielectric structure of FIG. 1(e). The structure of FIG. 1(b) includes a metal-nitride cap layer 18 designed to serve as a protective layer to facilitate the annealing process that results in the formation of a metal silicide layer 20 which is interdiffused with the Si_3N_4 layer of FIG. 1(e). Neither layer 18 nor substrate 12 serves as a capacitor plate. The structure of FIG. 1(b) is therefore not usable as a capacitor in the context of semiconductor integrated circuits and as such does not anticipate Applicant's claims to a capacitor.

As to the capacitor illustrated in FIG. 2(a) of Bronner, the dielectric layer in the capacitor is the specific composite dielectric structure illustrated in FIG. 1(e), which as discussed above is not included in Applicant's claimed invention.

Accordingly, Applicant requests withdrawal of the rejection of the above-cited claims by Bronner under 35 USC § 102(a).

C. U.S. Patent No. 5,960,294 to Zahurak

Claims 19, 53, 79-81, 85-87, 104, 106, 107, 108, 111-114 and 117-118 were rejected under 35 USC § 102(a) as being anticipated by Zahurak, et al. (U.S. Patent No. 5,960,294). Examiner cites col. 5, lines 45-52 as support for a metal oxide as being one of the possible materials for forming dielectric layer 24. In fact, the cited language in the specification makes no mention of metal oxides. Specifically, the statement that the dielectric layer "can be made of various materials such as silicon nitride, silicon dioxide, tantalum, barium, strontium titanate, combinations thereof, and the like" cannot reasonably be said to include metal oxides. This precludes a rejection of the claims based on anticipation under 35 USC § 102(a). Accordingly, Applicant requests that the anticipation rejection under 35 USC § 102(a) of the above-identified claims by Zahurak be withdrawn.

Product by process limitations

Examiner states that the limitations in claims 98-102 and certain limitations in claims 19, 20, 53 and 104-106 are taken as product by process limitations.

Applicant submits that for the reasons explained above in connection with the rejections based on Yoshida, Bronner and Zahurak, the above-identified claims describe a product that differs significantly from products in the cited prior art. Accordingly, Applicant respectfully requests reconsideration of the above-identified claims and withdrawal of the rejection of these claims.

§103 Rejection of the Claims

Claims 20, 82-84, 105, 109, 110, 115 and 116 were rejected under 35 USC § 103(a) as being unpatentable over Zahurak. Further, claims 20, 82-84, 105, 109, 110, 115 and 116 were rejected under 35 USC § 103(a) as being unpatentable over Bronner. Also, claims 98-102 were rejected under 35 USC § 103(a) as being unpatentable over Bronner in view of Jost, et al. (U.S. Patent No. 5,563,089) (hereinafter, "Jost").

The rejection of the above-identified claims is based on the presumption that Zahurak and Bronner each teach or render obvious all the limitations of claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114 and 117-118. However, Applicant has amended claims 19, 20, 79, 82, 85, 104-

106, 113, 115 and 117, and has explained in detail above why Zahurak and Bronner do not each teach or suggest all the limitation of these claims. Specifically, Bronner discloses a dielectric stack configuration that is not claimed in Applicant's invention, while Zahurak simply does not disclose the metal oxide dielectric layer that constitutes part of Applicant's claimed capacitor.

Accordingly, Applicant respectfully submits that the above-identified claims cannot be rejected for obviousness based on Zahurak combined with ordinary skill in the art, or alternatively based on Bronner combined with ordinary skill in the art . Applicant therefore respectfully requests that the rejections of the above-identified claims for obviousness under 35 USC § 103(a) be withdrawn.

CONCLUSION

Applicant respectfully requests reconsideration of the claims and withdrawal of the rejections of the claims. Applicant submits that the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joseph Gortych, at (802) 660-7199 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 20 day of August, 2001.

Tina Pugh
Name

_____
Signature

Docket No. 303.455US3 Micron Ref. No. 95-0505.02
WD # 353042

CLEAN VERSION OF PENDING CLAIMS

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION
Applicant: Karl M. Robinson
Serial No.: 09/470,265

Claims 19, 20, 53, 79-87, 98-102, and 104-124, as of August 20, 2001 (Date of Response to Final Office Action).

19. (Twice Amended) A capacitor, comprising:

a first conductive capacitor plate of a first material;

a second conductive capacitor plate; and

a dielectric interposed between said first and second conductive capacitor plates, wherein said dielectric is an oxide of a metal layer of a second material overlying the first conductive capacitor plate.

20. (Twice Amended) A memory system, comprising:

a monolithic memory device, comprising a capacitor, wherein the capacitor comprises:

a first conductive capacitor plate;

a second conductive capacitor plate; and

a dielectric interposed between said first and second conductive capacitor plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive capacitor plate; and

a processor configured to access the monolithic memory device.

53. A capacitor comprising:

a first capacitor electrode;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode; and

a second capacitor electrode.

79. (Once Amended) The capacitor of claim 19, wherein the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

80. The capacitor of claim 79, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

81. (Once Amended) The capacitor of claim 19, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

82. (Once Amended) The memory system of claim 20, wherein the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

83. The memory system of claim 82, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

84. (Once Amended) The memory system of claim 20, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

85. (Once Amended) The capacitor of claim 53, wherein the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

86. The capacitor of claim 85, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

87. The capacitor of claim 53, wherein the second capacitor electrode is formed from a material selected from the group consisting of polysilicon and metal.

98. A capacitor formed by a process comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose a portion of the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer to overly the polysilicon layer, the metal layer being formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing at least a portion of the metal layer to form a metal oxide to function as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

99. The capacitor of claim 98, wherein the electrolytic solution is a basic solution.

100. The capacitor of claim 98, wherein the electrolytic solution is an acidic solution.

101. The capacitor of claim 98, wherein the electrolytic solution is a solution of one part NH_4OH to ten parts water.

102. The capacitor of claim 98, wherein the electrolytic solution is a 0.1 molar solution of $HClO_4$.

104. (Twice Amended) A capacitor, comprising:

a first conductive plate serving as a first electrode of the capacitor;

a second conductive plate serving as a second electrode of the capacitor, the second conductive plate formed from a material selected from the group consisting of polysilicon and metal; and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

105. (Twice Amended) A memory system, comprising:

a monolithic memory device comprising a capacitor, wherein the capacitor comprises

a first conductive capacitor plate,

a second conductive capacitor plate formed from a material selected from the group consisting of polysilicon and metal, and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a processor configured to access the monolithic memory device.

106. (Twice Amended) A capacitor comprising:

a first capacitor electrode comprising polysilicon;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode , the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a second capacitor electrode formed from a material selected from the group consisting of polysilicon and metal.

107. The capacitor of claim 19, wherein the metal layer comprises titanium.

108. The capacitor of claim 19, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

109. The memory system of claim 20, wherein the metal layer comprises titanium.

110. The memory system of claim 20, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

111. The capacitor of claim 53, wherein the metal layer comprises titanium.

112. The capacitor of claim 53, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.

113. (Once Amended) The capacitor of claim 104, wherein the first conductive plate comprises polysilicon having a thickness of 200 to 400 Angstroms.

114. The capacitor of claim 104, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

115. (Once Amended) The memory system of claim 105, wherein the first conductive capacitor plate comprises polysilicon.

116. The memory system of claim 105, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

117. (Once Amended) The capacitor of claim 106, wherein the first capacitor electrode has a thickness from 200 to 400 Angstroms.

118. The capacitor of claim 106, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.

119. (New) A capacitor structure formed on a substrate, comprising:

a first conductive capacitor plate formed atop the substrate;

a first metal layer formed atop the first conductive capacitor plate;

a first metal oxide layer formed from the metal layer such that the remaining first metal layer forms part of the first conductive capacitor plate; and

a second conductive layer formed atop the first metal oxide layer.

120. (New) The capacitor structure of claim 119, further including:

a second metal layer formed atop the second conductive layer;

a second metal oxide layer formed from the second metal layer such that the remaining second metal layer forms part of the second conductive layer;

a third conductive layer formed atop the second metal oxide layer, wherein the first and second metal oxide layers and the second conductive layer form the dielectric of the capacitor and the third conductive layer serves as a second conductive capacitor plate.

121. (New) The capacitor structure of claim 119, wherein:

the first conductive capacitor plate comprises polysilicon and the first metal layer comprises a metal selected from the group of metals consisting of titanium, tungsten, copper, gold, and nickel.

122. (New) The capacitor of claim 119, wherein the first metal layer is substantially completely oxidized to form the metal oxide layer.

123. (New) The capacitor of claim 119, wherein the first metal oxide layer has a thickness of between 10 and 1000 Angstroms.

124. (New) The capacitor of claim 119, wherein the first metal layer is alloyed with another material.